

What is claimed is:

1. A processor comprising:

a processor core including a general-purpose register, an instruction decoder, and a second
5 execution unit;

an extension unit including a first execution unit connected to the processor core; and

a direct memory access controller connected to both the processor core and the extension unit.

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2. The processor of claim 1, further comprising a control bus connected to the processor core and the extension unit.

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3. The processor of claim 2, further comprising a clock disable signal generation circuit organized to receive an extended instruction code from the instruction decoder and outputs a clock disable signal.

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4. The processor of claim 3, further comprising a clock gating circuit organized to receive the clock disable signal and transmits a signal for halting a clock signal for the processor core.

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5. The processor of claim 4, wherein the clock

disable signal halts the clock signal for the processor core.

6. The processor of claim 2, further comprising a
5 halt request signal generation circuit organized to receive an extended instruction code from the instruction decoder and transmit a halt request signal to the processor core.

10 7. The processor of claim 2, wherein the first execution unit is a reconfigurable first execution unit.

8. The processor of claim 7, wherein the extension
15 unit further comprises an instruction decoder, a control register, and local memory.

9. The processor of claim 7, wherein the instruction decoder in the extension unit further comprises a
20 reconfigurable logic circuit that is the same as the reconfigurable first execution unit.

10. The processor of claim 7, wherein configuration data provided to the reconfigurable logic circuit,
25 is provided through data transmission from the direct access memory controller via a configuration

interface connecting the reconfigurable first execution unit in the extension unit and the direct memory access controller.

5 11. The processor of claim 8, wherein configuration data provided to the reconfigurable logic circuit is stored in the internal local memory of the extension unit.

10 12. A semiconductor integrated circuit, comprising:

a semiconductor chip;

a processor core integrated on the semiconductor chip including a general purpose register, an instruction decoder, and a second execution unit;

an extension unit integrated on the semiconductor chip including a first execution unit connected to the processor core;

20 a direct memory access controller integrated on the semiconductor chip and connected to both the processor core and the extension unit.

13. The semiconductor integrated circuit of claim 25 12, further comprising a control bus integrated on the semiconductor chip and connected to both the

processor core and the extension unit.

14. The semiconductor integrated circuit of claim
13, further comprising a clock disable signal
5 generation circuit integrated on the semiconductor
chip and is organized to receive an extended
instruction code from the instruction decoder and
outputs a clock disable signal.

10 15. The semiconductor integrated circuit of claim
14, further comprising a clock gating circuit
integrated on the semiconductor chip and is
organized to receive the clock disable signal and
transmits a signal for halting a clock for the
15 processor core to the processor core.

16. The semiconductor integrated circuit of claim
13, further comprising a halt request signal
generation circuit integrated on the semiconductor
20 chip and is organized to receive an extended
instruction code from the instruction decoder and
transmit a halt request signal to the processor
core.

25 17. The semiconductor integrated circuit of claim
13 wherein the first execution unit is a

reconfigurable first execution unit.

18. The semiconductor integrated circuit of claim
17, wherein the instruction decoder in the
5 extension unit further comprises a reconfigurable
logic circuit that is the same as the reconfigurable
first execution unit.

19. The semiconductor integrated circuit of claim
10 17, wherein configuration data provided to the
reconfigurable logic circuit, is provided through
data transmission from the direct access memory
controller via a configuration interface
connecting between the reconfigurable first
15 execution unit in the extension unit and the direct
memory access controller.

20. The semiconductor integrated circuit of claim
17, wherein configuration data provided to the
20 reconfigurable logic circuit is stored in the
internal local memory of the extension unit.